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NEW APPLICATION TRANSMITTAL - UTILITY

Sir:

Transmitted herewith for filing is a **utility** patent application:

Inventor(s): Arun Jayaraman

Title: SYSTEM AND METHOD OF FREQUENCY SYNTHESIS TO AVOID GAPS AND VCO PULLING IN DIRECT BROADCAST STATELITE SYSTEMS

I. PAPERS ENCLOSED HEREWITH FOR FILING UNDER 37 CFR § 1.53(b):

23 Page(s) of Written Description

5 Page(s) Claims

1 Page(s) Abstract

5 Sheets of Drawings ☐ Informal ☒ Formal

II. ADDITIONAL PAPERS ENCLOSED IN CONNECTION WITH THIS FILING:

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☒ Power of Attorney ☐ Separate ☒ Combined with Declaration

☒ Assignment to Conexant Systems, Inc. and assignment cover sheet

☐ Verified Statement establishing **"Small Entity"** under 37 CFR §§ 1.9 and 1.27

☐ Priority Document No(s): _____

☐ Information Disclosure Statement w/PTO 1449 ☐ Copy of Citations

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Respectfully submitted,

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Dated: 6/6/00

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Multiple Dependent Claims	$260	(if applicable)				☐	$0.00
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SYSTEM AND METHOD OF FREQUENCY SYNTHESIS TO AVOID GAPS AND VCO PULLING IN DIRECT BROADCAST STATELITE SYSTEMS

Inventor: Arun Jayaraman

Background of the Invention

1. Related Application

The following application of common assignee contains some common disclosure as the present application and is incorporated herein by reference in its entirety:

U.S. Patent Application entitled "FULLY INTEGRATED BROADBAND TUNER", filed February 4, 2000, Application Serial No. 09/497,717.

2. Field of the Invention

The present invention relates generally to broadcast receivers, and more particularly to broadband tuners utilizing a local oscillator.

3. Related Art

Broadcast satellites transmit signals over multiple channels across a broadband spectrum. These satellites use standardized broadcast formats, such as Digital Satellite Service (DSS), used in North America, and Direct Video Broadcast (DVB), used in Europe. Both DSS and DVB broadcast over a broadband spectrum ranging from 12 to 14 GHz. When combined with receiving systems, these broadcast satellites create a direct broadcast satellite system (DBS).

A DSS/DVB receiving system generally includes an antenna, a low-noise block down-converter (LNB) and a down-conversion broadband receiver. Although there are many ways in which to implement the down-conversion broadband receiver, a direct down-conversion broadband

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receiver implementation is the most common in current generation tuners. The direct down-conversion broadband receiver comprises a direct down-conversion tuner and a baseband demodulator.

The LNB converts the 12-14 GHz band signal received by the antenna into a 950 – 2150 MHz band signal. This broadband signal is specified by the DSS/DVB standards. The direct down-conversion tuner directly converts one channel in this 950 – 2150 MHz band down to baseband, which consists of in-phase (I) and quadrature (Q) components. These I and Q components are then converted into digital data and demodulated by the baseband demodulator.

The direct down-conversion tuner in the direct down-conversion broadband receiver typically utilizes mixers to perform the down-conversion from 950 – 2150 MHz to I and Q components. These mixers require a local oscillator (LO), which typically comprises a frequency synthesizer with a step size equal to a receive-channel spacing. Such local oscillators are commonly implemented using a reference frequency generator, at least one voltage controlled oscillator (VCO), and a phase-locked loop (PLL) comprising a phase/frequency detector (PFD), a charge pump, a loop filter, and a divider. The reference frequency generator uses an external crystal.

Although the term "local oscillator" is frequently used to refer to only a VCO portion of a frequency synthesizer within a tuner, as used herein, the local oscillator refers to the frequency synthesizer within the tuner.

The signal from this local oscillator drives the mixers. By definition, the mixers in the direct down-conversion broadband receiver are driven by an input frequency that is equivalent to the carrier frequency of a selected channel. Thus the conversion to baseband is done in one step, thereby making it a direct down-conversion. Typically, the local oscillator operates at this same frequency input to the mixers.

However, some local oscillators are designed to operate at approximately twice the frequency of the carrier signal. The output of the local oscillator is then put through a 2-divider just prior to being fed to the mixers. This is done to avoid the many problems, such as cross modulation and direct current (DC) offset, which arise when the local oscillator operates at exactly the same frequency as the carrier.

In addition, when the signal is to be separated into I and Q components, using this divide by two approach offers another benefit. The 2-divider can be designed to easily generate the phase shift required to obtain the Q component, thereby avoiding the need for poly-phase filters or other complex designs. Thus with a 2-divider approach to the direct down-conversion tuner in a direct-down conversion receiver, both the I and Q components are obtained simultaneously, with a high degree of accuracy.

However, in DBS systems, the 2-divider approach is problematic. A DSS/DVB receiver must be able to receive channels over the entire broadband spectrum defined by the DSS/DVB standards. This broadband receiving spectrum causes the typical 2-divider approach to tuner design to create undesirable coupling between the local oscillator (LO) signal and the incoming radio frequency (RF) signal, within a DBS tuner chip. If the RF signal at twice a desired receive channel frequency is strong, this coupling can cause VCO pulling.

In addition, the RF signal at twice the desired receive channel frequency can mix with the LO signal and cause signal-to-noise-ratio degradation. For example, because the VCO typically generates a waveform, which is not a perfect sine wave, this generated waveform has additional harmonic content. These harmonic overtones can lead to composite triple beat. Thus, when some of the lower frequencies in the broadband spectrum of the DBS system are tuned to, the VCO wave

form can interfere with higher RF channels, which in turn can created a product on the channel being tuned to, thereby reducing sensitivity of the tuner chip from the front end.

In addition to this VCO pulling problem with current broadband receivers, typical broadband receivers also consume an undesirable amount of power. With the DSS/DVB standards, the channel can be at any frequency in the specified signal range of 950 to 2150 MHz. A tuner chip designed to directly convert this broadband spectrum down to baseband typically relies on a reference frequency of 1 MHz or 500 KHz. The reference frequency used will commonly be set equal to a receive-channel spacing for the particular application. Generally, the reference frequency will not deviate significantly from these values. The reason for this is twofold. First, as the reference frequency is lowered, the phase noise performance required of the PLL increases, because the multiplication factor to the output becomes higher. Second, as the reference frequency is raised, the tuner chip loses granularity.

Because the tuning spectrum in DBS systems is so wide and any frequency in that range may be a channel, typical DBS tuner chips utilize a 16/17 prescaler in the divider in the PLL in order to handle the 1 MHz reference frequency case. This is done to avoid gaps in tuning range caused by a prescaler with too high of a modulus ratio. However, the use of a lower modulus prescaler in the tuner chip requires operation of counters in the divider at a higher frequency. Thus, this approach to local oscillator design creates a significant and undesirable power drain.

Therefore, what is needed is a system and method for local oscillator design for use in a broadband tuner, which avoids gaps in tuning range and VCO pulling, while also reducing the broadband tuner's power consumption.

Summary of the Invention

The present invention is directed toward a system and method for designing a broadband tuner.

The present invention provides a method for dividing a broadband spectrum into sub-bands, thereby enabling the design of a broadband tuner with reduced VCO pulling. By splitting up a broadband spectrum and introducing various multipliers, the present invention allows a local oscillator within a broadband tuner to always generate signals that lie outside of the broadband spectrum for a particular broadband application. In this fashion, VCO pulling within the broadband tuner is reduced.

In addition, according to one aspect of the invention, the broadband tuner has reduced power consumption. Because the broadband spectrum is broken up into sub-bands and multipliers are introduced, additional power savings within the broadband tuner are possible. The present invention provides a system and method for maximizing a modulus ratio for a dual modulus prescaler within the local oscillator, without introducing gaps in frequency coverage. In this fashion, the present invention reduces the number of high frequency components within the broadband tuner, thereby reducing power consumption.

Further features and advantages of the invention as well as the structure and operation of various embodiments of the invention are described in detail below with reference to the accompanying drawings.

Brief Description of the Figures

FIG. 1 is a block diagram depicting an example operational environment according to one embodiment of the present invention;

FIG. 2 is a block diagram depicting additional detail regarding one aspect of an example operational environment according to one embodiment of the present invention;

FIG. 3 is a block diagram depicting components of a direct down-conversion tuner chip according to one embodiment of the present invention;

FIG. 4 is a block diagram depicting components of a local oscillator with an N-divider and related elements of a broadband receiver system according to one embodiment of the present invention; and

FIG. 5 is a two-part flow chart, and a block diagram of an exemplary broadband spectrum, depicting a method for providing a broadband tuner utilizing sub-bands according to one embodiment of the present invention.

Detailed Description of the Invention

The present invention is directed toward a system and method for designing a broadband tuner. The present invention is disclosed and described herein in terms of an example DBS embodiment. However, after reading this description it will become apparent to one skilled in the art how to implement the invention in alternative embodiments and alternative applications. As such, the description of this example embodiment should not be construed to limit the scope or breadth of the present invention.

FIG. 1 is a block diagram depicting an example operational environment according to one embodiment of the present invention. Referring now to Fig. 1, a broadcast satellite 100 transmits a signal comprising multiple channels over a broadband spectrum covering 12 to 14 GHz. The signal is received by an antenna 104. The signal is then passed through a low-noise block converter (LNB) 108, which takes the 12-14 GHz band signal received by the antenna 104 and converts it to a 950-2150 MHz band signal.

The signal then passes through a coax cable 112 into a set-top box 116, which allows a user to select a channel to view. Set-top box 116 contains other features and functions well understood by those skilled in the art and not essential to the disclosure of the present invention. Set-top box 116 also contains a direct down-conversion receiver 200. In one embodiment, the direct down-conversion receiver 200 generates data that is sent to a decoder 120. The decoder 120 is an MPEG decoder in one embodiment, and its output is sent to a television 124, or other DBS display device, for viewing by a user.

FIG. 2 is a block diagram depicting additional detail regarding one aspect of an example operational environment according to one embodiment of the present invention. Referring now to Fig. 2, the direct down-conversion receiver 200 is the same as that shown in Fig. 1. It has an input

208, which is the incoming signal from the LNB 108. It also has an output 236, which is the data sent to the decoder 120.

The direct down-conversion receiver 200 includes a direct down-conversion tuner 204 and a demodulator 232. The direct down-conversion tuner 204 outputs I and Q components 220 and 224. These I and Q components 220 and 224 are at baseband. The demodulator 232 takes these I and Q components 220 and 224, and converts them to digital output in a manner well known by those skilled in the art.

In one embodiment of the present invention, the direct down-conversion tuner 204 comprises a tuner chip 300, a crystal 212 and a loop filter 216. The crystal 212 provides the tuner chip 300 with a crystal reference frequency in a manner well known in the relevant art(s). In one embodiment, crystal 212 is a 10.11 MHz crystal. Also in one embodiment, the tuner chip 300 has a lock detect output 228 that is fed to the demodulator 232. In an alternative embodiment, lock detect output 228 is not an output, but is used instead entirely within tuner chip 300.

In one embodiment, loop filter 216 is a low-pass filter provided for use with a phase-locked loop inside tuner chip 300 in a manner well known in the relevant art(s). In addition, alternative embodiments include those having loop filter 216 contained within tuner chip 300.

While the present invention is disclosed in terms of a direct down-conversion receiver used as part of a DBS intermediate frequency (IF) receiver system, those skilled in the relevant art(s) will understand that the present invention is applicable to any broadband application in which twice a lowest potential channel is a frequency within the broadband spectrum.

FIG. 3 is a block diagram depicting components of a direct down-conversion tuner chip according to one embodiment of the present invention. Referring now to Fig. 3, the direct down-conversion tuner chip 300 comprises multiple inputs, outputs and components. RF input 304 is the

RF signal from the LNB 108. In one embodiment, RF input 304 is provided on two balanced pins. Automatic gain control (AGC) input 308 is a DC voltage that, in one embodiment, controls the gain of RF attenuator 340 and AGC amplifiers 370, 372, 378 and 380. Crystal reference frequency input 312 is the input from the crystal 212.

Check reference output 316 provides the reference clock for the demodulator 232 in a manner well known in the relevant art(s). I output 220 is the in-phase component of a selected channel. Q output 224 is the quadrature component of the selected channel. In one embodiment, loop filter output 390 connects to loop filter 216, thus providing a loop filter component of the PLL within a local oscillator 400. Finally, in one embodiment lock detect output 228 is provided for use with the demodulator 232 as discussed previously.

Logic interface 332 is coupled to the local oscillator 400 and to a 2/4 divider-shifter 362. This coupling enables logic interface 332 to control the behavior of both the local oscillator 400 and the 2/4 divider-shifter 362 in a manner described herein. Logic interface 332 includes digital storage registers as needed. Those skilled in the relevant art(s) will understand when and how many such digital storage registers are needed given the disclosure herein and the particular application. In one embodiment, logic interface 332 is controlled via a three-line bus. This three-line bus comprises a serial bus clock signal 320, a serial bus latch enable 324 and a serial bus data line 328.

AGC Control 344 splits the incoming AGC input 308 such that it is provided to multiple components within the direct down-conversion tuner chip 300. One such component is RF attenuator 340, which is a voltage controlled attenuator. In one embodiment, RF input 304 is provided to RF attenuator 340, which decreases the amplitude variations in the receive signal. This is done to optimize the spurious free dynamic range of the receiver for various input signal levels.

Local oscillator 400 feeds the mixers 358 and 360 via the 2/4 divider-shifter 362. In one embodiment, the output of the local oscillator 400 is selected to be exactly twice or four times the desired receive frequency. This is done to minimize the RF to LO coupling, as described in greater detail below. The output from the local oscillator 400 is then divided by an appropriate number in the 2/4 divider-shifter 362 before being fed to the mixers 358 and 360. Additionally, the 2/4 divider-shifter 362 shifts the phase of the signal provided to the mixer 360 by ninety degrees. This is done to obtain the quadrature component of the received signal.

The output of the mixers 358 and 360 is the difference in frequency between RF signal 304 and the oscillator signals from the 2/4 divider-shifter 362. Thus, when RF signal 304 and the oscillator signals from the 2/4 divider-shifter 362 have the same frequency, the RF is removed, thereby converting the signal to baseband. In one embodiment, the outputs of mixers 358 and 360 are then passed through two separate fixed low-pass filters 366 and 368, and two separate AGC amplifiers 370 and 372. The fixed low-pass filters 366 and 368 aid in tuning out any part of the RF signal not within the selected channel. The AGC amplifiers 370 and 372 maintain the signal of the selected channel at a constant amplitude, regardless of variations in the receive signal level. This is done to keep the signal amplitude within the narrow range required by the demodulator 232.

Also in one embodiment, DC offset cancellation components 348 and 352 bridge the fixed low-pass filters 366 and 368, and the AGC amplifiers 370 and 372 to cancel any DC offset for the I and Q channels. This is done because LO leaks to RF, mixed down to DC. If the DC offset is not cancelled, it will clip the amplifier chain. In one embodiment, DC offset cancellation components 348 and 352 are connected to two off-chip capacitors. However, alternative embodiments include other methods and apparatus for canceling DC offset, such as off-chip alternating current (AC) coupling via a series capacitor.

In one embodiment, variable low-pass filters 374 and 376 aid in tuning out any part of the RF signal not within the selected channel, thus ensuring consistent baseband output. In alternative embodiments, these variable low-pass filters 374 and 376 are fixed low-pass filters or other components able to help ensure a proper baseband output, such as off-chip L-C filters. AGC amplifiers 378 and 380 maintain the signal of the selected channel at a constant amplitude, regardless of variations in the receive signal level. This is done to keep the signal amplitude within the narrow range required by the demodulator 232 to maximize signal-to-noise-ratio.

As mentioned previously, the present invention is described herein in terms of this example DBS embodiment. However, it should be remembered that description in these terms is provided for ease of discussion only. After reading the description herein, it will become apparent to one skilled in the relevant art(s) that the present invention can be implemented in any of a number of alternative embodiments and alternative broadband applications. For example, although the disclosure provided herein shows the demodulator as separate from the tuner, the present invention may be implemented on a single integrated circuit with both the tuner and the demodulator on the same chip. As such, the description of the present invention in terms of this example embodiment should not be construed to limit the scope or breadth of the present invention.

FIG. 4 is a block diagram depicting components of a local oscillator with an N-divider and related elements of a broadband receiver system according to one embodiment of the present invention. Referring now to FIG. 4, the local oscillator 400 from Fig. 3 is now presented in greater detail. Crystal reference frequency input 312, clock reference output 316, loop filter output 390, and the lock detect output 228 are the same as described above. Likewise, the three-line bus for logic interface 332 is also the same, comprising the serial bus clock signal 320, the serial bus latch enable

324 and the serial bus data line 328. A local oscillator output 450 is the signal provided to the 2/4 divider-shifter 362, and thereby the mixers 358 and 360 on FIG. 3.

In one embodiment, logic interface 332 is coupled to a divide by R block 408, an N-divider 430, a programmable charge pump 416, and at least one voltage controlled oscillator (VCO) 424. In one embodiment, divide by R block 408 is included in LO 400 to allow the direct down-conversion tuner chip 300 the ability to be used in multiple broadband receiver applications. R is determined by the demodulator's ability to correct any frequency offsets. In one embodiment, in which crystal reference frequency input 312 is at 10.11 MHz, divide by R block 408 is programmed by logic interface 332 with two bits, and R will be either 10 or 20, depending on a reference frequency required by a particular broadband receiver application. The reference frequency is 1 MHz or 500 kHz respectively.

Phase/frequency detector (PFD) 412 and charge pump 416 are standard components of a phase-locked loop and function in a manner well known in the relevant art. The lock detect output 228 is created by lock detect logic 420. This lock detect logic 420 is a standard component of phase-locked loops and may be implemented in different ways in alternative embodiments. For example, in one embodiment a simple nor-gate can be placed across outputs of the PFD 412.

In one embodiment, loop filter output 390 attaches between charge pump 416 and the at least one VCO 424. Loop filter output 390 connects to loop filter 216, thus converting the current output from charge pump 416 into a voltage output for driving one of the at least one VCO 424 at a time. In alternative embodiments, different PLL architectures are used. For example, the present invention may be implemented with a fractional-N PLL or a multi loop PLL, instead of the PLL architecture disclosed herein.

N-divider 430 takes a local oscillator output 450 and divides it by an appropriate number N to provide a compare frequency input to the PFD 412. The appropriate number N is determined by a desired frequency derived from the selected channel. By dividing the local oscillator output by N, the PLL locks the local oscillator output 450 to the desired frequency, which is equal to N times the reference frequency. In one embodiment, the local oscillator output 450 is a sine wave. In an alternative embodiment, the local oscillator output 450 is a square wave.

In one embodiment, N-divider 430 comprises a fixed divide-by-2 block 432, a 32/33 prescaler 434, a 9-bit B-counter 436, and a 5-bit A-counter 438. N-divider 430 is programmed via logic interface 332 by loading registers in the 9-bit B-counter 436 and the 5-bit A-counter 438, thereby causing the at least one VCO 424 to lock onto the desired frequency. N is an integer, which is determined by a B-number and an A-number calculated using the following equations:

(1) $\text{B-number} = \lfloor (\text{the desired frequency} \div 32 \div 2) \rfloor$

(2) $\text{A-number} = \lfloor (\text{the desired frequency} \div 2) - (32 \bullet \text{B-number}) \rfloor$

Once the B-number and the A-number are loaded into the 9-bit B-counter 436 and the 5-bit A-counter 438 respectively, the N-divider 430 operates by dynamically changing a modulus control bit for the 32/33 prescaler 434. For A-number of clock cycles, the N-divider 430 divides the local oscillator output 450 by 33, and for (B-number –A-number) of clock cycles, the N-divider 430 divides the local oscillator output 450 by 32.

In one embodiment, the desired frequency is either two or four times the selected channel's frequency. A selected frequency identifier 470 determines the desired frequency based upon the selected channel and two frequency sub-bands that make up the broadband spectrum. If the selected channel falls in a first-band of the two frequency sub-bands, the desired frequency is set to four times

the selected channel's frequency, and the 2/4 divider-shifter 362 divides the local oscillator output 450 by four before inputting it to the mixers. If the selected channel falls in a second-band of the two frequency sub-bands, the desired frequency is set to two times the selected channel's frequency, and the 2/4 divider-shifter 362 divides the local oscillator output 450 by two before inputting it to the mixers.

In one embodiment, the first-band covers the frequency range 950 – 1075 MHz, and the second-band covers the frequency range 1076 – 2150 MHz. The selected frequency identifier 470 determines the desired frequency, calculates the B-number and the A-number using equations (1) and (2) above, loads the B-number into the 9-bit B-counter 436 via the logic interface 332, loads the A-number into the 5-bit A-counter 438 via the logic interface 332, and sets a divider-state for the 2/4 divider-shifter 362 via the logic interface 332.

In alternative embodiments, there are more than two sub-bands. In addition, alternative embodiments include additional frequency ranges for the sub-bands, provided that the desired frequency never lies in the broadband spectrum. Those skilled in the relevant art(s) will understand how to implement these alternative embodiments given the disclosure herein.

The selected frequency identifier 470 may be implemented using hardware, software or a combination thereof and may be implemented in a computer system or other processing system. In one embodiment, the selected frequency identifier 470 is implemented in a software driver running on a general purpose computer. However, alternative embodiments include multiple software environments and/or multiple hardware designs, all of which perform the functionality described herein.

FIG. 5 is a two-part flow chart, and a block diagram of an exemplary broadband spectrum, depicting a method for providing a broadband tuner utilizing sub-bands according to one

embodiment of the present invention. Referring now to FIG. 5, the process begins with step 500, in which a particular broadband application is selected for the broadband tuner. The particular broadband application defines a broadband spectrum 540 having an upper limit 590 and a lower limit 550 for the frequencies that can contain receivable channels. In one embodiment, the particular broadband application is the DBS system, and the upper limit 590 and the lower limit 550 are 2150 MHz and 950 MHz respectively. However, the present invention is applicable to all broadband applications in which twice the lower limit 550 is less than the upper limit 590.

Following step 500, one or more cut-off frequencies are identified in step 504. The cut-off frequencies are identified in step 504 based on the upper limit 590 and the lower limit 550. Steps 520 through 532 depict an exemplary process for identifying the cut-off frequencies. These steps are discussed further below.

In step 508, one or more terminal frequencies are selected based upon the cut-off frequencies. In one embodiment, the terminal frequencies are equal to a channel frequency just above each of the cut-off frequencies. Thus, in one DBS embodiment, the cut-off frequency is 1075 MHz, and the terminal frequency is 1076 MHz, when the channel frequencies are at 1 MHz intervals. However, alternative embodiments include those in which the terminal frequencies are any frequency greater than each of the cut-off frequencies and less than either the upper limit 590 or a previous terminal frequency.

Following step 508, the broadband spectrum 540 is divided into sub-bands in step 512 using the terminal frequencies selected in step 508. A first-band extends from the lower limit 550 to a channel frequency just below a first-terminal from the terminal frequencies. A last-band extends from a last-terminal from the terminal frequencies to the upper limit 590. Any intermediate bands

extend from each respective terminal from the terminal frequencies to a channel frequency just below a next-terminal from the terminal frequencies.

Step 516 is the step of designing a new broadband tuner using the sub-bands created in step 512. The new broadband tuner is designed in step 516 in the same fashion as the broadband tuner disclosed herein. The new broadband tuner includes a variable state divider that divides by different numbers for the sub-bands. The different numbers are defined by various multipliers used to identify the cut-off frequencies in step 504. In addition, the new broadband tuner includes a P/P+1 prescaler in which P is maximized without introducing gaps in frequency coverage given a range of potential desired frequencies defined by the channel frequencies, the sub-bands and the various multipliers.

This maximization of P is done using standard mathematical formulas for calculating the available frequencies given a particular prescaler, a particular A-counter and a particular B-counter. A standard N-divider, such as disclosed herein, is limited by two key factors: (1) the particular A-counter must have a number of input bits equal to $\log_2(P)$; (2) a B-number loaded onto the particular B-counter must be greater than any A-number loaded onto the particular A-counter, or the standard N-divider circuit will fail.

Thus, for example, a standard N-divider with a 32/33 prescaler cannot generate a 991 MHz input to the mixers in a traditional divide-by-two scheme using a 1 MHz reference frequency. Using equations (1) and (2) above, if a desired frequency is 1982 MHz (twice a selected channel frequency):

$$\text{B-number} = \lfloor (\text{the desired frequency} \div P \div 2) \rfloor = \lfloor (1982 \div 64) \rfloor = 30$$

$$\text{A-number} = \lfloor (\text{the desired frequency} \div 2) - (P \bullet \text{B-number}) \rfloor = \lfloor (991 - 32 \bullet 30) \rfloor = 31$$

These are invalid values for B-number and A-number. Thus in the present invention, a 32/33 prescaler cannot be used if 991 MHz is in the range of potential desired frequencies defined by the channel frequencies, the sub-bands and the various multipliers.

By maximizing P using the standard mathematical formulas, given the range of potential desired frequencies to be generated, the present invention reduces power consumption for the new broadband tuner. During this maximizing process, which is part of step 516, steps 508 through 512 can be repeated to arrive at alternative terminal frequencies and sub-bands, thereby enabling additional power consumption benefits. A person of skill in the relevant art(s) will understand how to implement this maximization process given the disclosure herein.

Steps 520 through 532 depict an exemplary process for identifying the cut-off frequencies. The process begins with step 520 in which a multiplier is set to two. In step 524, the lower limit 550 from the broadband spectrum 540 is multiplied by the multiplier and compared with the upper limit 590. If the lower limit 550 times the multiplier is less than the upper limit 590, the process proceeds to step 528. Otherwise, the process ends.

In step 528, a next cut-off is set to the upper limit 590 divided by the multiplier. On a first pass through step 528, the next cut-off is a first-cut-off 570. On a second pass, the next cut-off is a second-cut-off 560. On a third pass, it is a third-cut-off 555, etc. Following step 528, the multiplier is increased by a factor of two in step 532, before the process returns to step 524.

While various embodiments of the present invention have been described above, it should be understood that they have been presented by way of example only, and not limitation. Thus, the breadth and scope of the present invention should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

What is claimed is:

1. In a broadband tuner for use in a broadband receiver, a system for generating selectable signals for tuning, the system comprising:

a divider-shifter that divides and shifts a local oscillator signal to obtain in-phase and quadrature components of a selected channel frequency, wherein said divider-shifter divides the local oscillator signal by a first-number when the selected channel frequency is within a first-band, and wherein said divider-shifter divides the local oscillator signal by a second-number when the selected channel frequency is within a second-band;

an N-divider that divides the local oscillator signal by a value N before comparison with a reference frequency, thereby enabling a current frequency of the local oscillator signal to be locked to the value N multiplied by the reference frequency, said N-divider comprising:

an A-counter that counts an A-number of clock cycles;

a B-counter that counts a B-number of clock cycles, said B-counter being coupled with said A-counter; and

a dual modulus P/P+1 prescaler having a P-number, said dual modulus P/P+1 prescaler coupled with said A-counter and said B-counter such that for the A-number of clock cycles said N-divider divides the local oscillator signal by a value one greater than the P-number, and for a number of clock cycles equal to the B-number minus the A-number said N-divider divides the local oscillator signal by the P-number; and

a selected frequency identifier that determines whether the selected channel frequency falls within the first-band or the second-band, causes said divider-shifter to divide by an appropriate number, and programs the value N such that the current frequency of the local oscillator signal is equal to the first-number times the selected channel frequency when the selected channel frequency falls within the first-band and the current frequency of the local oscillator signal is equal to the

second-number times the selected channel frequency when the selected channel frequency falls within the second-band.

2. The system of claim 1, wherein the P-number is maximized without introducing gaps in frequency coverage given a range of potential frequencies for the current frequency.

3. The system of claim 2, wherein said selected frequency identifier causes said divider-shifter to divide by the appropriate number, and programs the value N, via a logic interface, said system further comprising:

said logic interface coupled with said divider-shifter such that the appropriate number is specifiable via said logic interface, and said logic interface is coupled with said N-divider such that said logic interface enables loading of the A-number and the B-number, thereby enabling programming of the value N.

4. The system of claim 3, wherein the reference frequency is derived by dividing a crystal reference frequency by a value R, said system further comprising:

an R-divider coupled with said logic interface such that said logic interface enables programming of the value R, said R-divider designed to divide the crystal reference frequency by the value R to obtain the reference frequency.

5. The system of claim 3, wherein the reference frequency is 1.011 MHz.

6. The system of claim 3, wherein said N-divider further comprises a fixed 2-divider coupled with said dual modulus P/P+1 prescaler.

7. The system of claim 6, wherein the first-number is four and the second-number is two.

8. The system of claim 7, wherein the first-band is nine hundred and fifty MHz to one thousand and seventy five MHz, and the second-band is one thousand and seventy six MHz to two thousand one hundred and fifty MHz.

9. The system of claim 8, wherein the P-number is thirty two, said A-counter further comprises five input register pins for storing A-numbers ranging from zero to thirty-one, and said B-counter further comprises nine input register pins for storing B-numbers ranging from zero to

five hundred and eleven.

10. A method for providing a broadband tuner for use in a broadband receiver comprising the steps of:

selecting a particular application for a broadband tuner such that an upper limit and a lower limit for carrier frequencies from a broadband spectrum are predefined;

identifying a cut-off frequency between the upper limit and the lower limit, the cut-off frequency being equal to the upper limit divided by a multiplier;

selecting a terminal frequency corresponding to the cut-off frequency, the terminal frequency being equal to a channel greater than the cut-off frequency for the particular application;

dividing the broadband spectrum into at least two sub-bands having at least two corresponding multipliers, wherein the at least two sub-bands are defined by the lower limit, the terminal frequency, and the upper limit, and wherein the multiplier is one of the at least two corresponding multipliers; and

designing the broadband tuner such that it comprises:

a local oscillator capable of generating a signal equal to a selected channel frequency times one of the at least two corresponding multipliers, wherein the one of the at least two corresponding multipliers is determined by which of the at least two sub-bands encompasses the selected channel frequency; and

a divider capable of dividing the signal by the one of the at least two corresponding multipliers.

11. The method of claim 10, wherein said designing step further comprises the step of designing the local oscillator such that it comprises a dual modulus P/P+1 prescaler having a P-number which is maximized without introducing gaps in frequency coverage given a range of potential frequencies for the signal.

12. The method of claim 11, wherein the P-number is thirty two.

13. The method of claim 10, wherein the at least two corresponding multipliers are powers of two.

14. The method of claim 13, wherein the divider is also capable of shifting the signal, thereby enabling generation of in-phase and quadrature components during down-conversion.

15. The method of claim 10, wherein the cut-off frequency is one and only one cut-off frequency.

16. In a broadband tuner for use in a broadband receiver, a system for generating selectable signals for tuning, the system comprising:

means for identifying a current band in which a selected channel frequency falls, the current band being one of at least two frequency bands covering a broadband spectrum;

means for generating a signal with a signal frequency equal to a multiplier times the selected channel frequency, wherein the multiplier is selected based upon the current band; and

a divider that divides the signal in preparation for down-converting an RF signal corresponding to the selected channel frequency to a baseband signal.

17. The system of claim 16, wherein said means for generating is a local oscillator with a dual modulus P/P+1 prescaler having a P-number.

18. The system of claim 17, wherein the P-number is maximized without introducing gaps in frequency coverage given a range of potential frequencies for the signal frequency.

19. The system of claim 18, wherein the P-number is thirty two.

20. The system of claim 16, wherein the multiplier is a power of two related to the current band such that the multiplier equals two to the power of a quantity, total frequency bands minus an integer-order for the current band, wherein the integer-order starts with zero for a lowest band from the at least two frequency bands.

21. In a tuner and receiver system for generating signals for tuning, the system comprising:

a frequency identifier that determines whether a channel frequency falls within a current band, the current band being one of at least two frequency bands covering a spectrum;

a frequency synthesizer having a dual modulus prescaler having a P-number, said frequency synthesizer capable of generating a first signal with a first signal frequency equal to a multiplier times the channel frequency, wherein the multiplier is selected based upon the current band; and

a divider that divides the first signal in preparation for converting a second signal corresponding to the channel frequency to a third signal.

22. The system of claim 21, wherein the P-number is maximized without introducing gaps in frequency coverage given a range of potential frequencies for the first signal frequency.

23. The system of claim 22, wherein the P-number is thirty two.

24. The system of claim 21, wherein the multiplier is a power of two related to the current band such that the multiplier equals two to the power of a quantity, total frequency bands minus an integer-order for the current band, wherein the integer-order starts with zero for a lowest band from the at least two frequency bands.

SYSTEM AND METHOD OF FREQUENCY SYNTHESIS TO AVOID GAPS AND VCO PULLING IN DIRECT BROADCAST STATELITE SYSTEMS

Abstract

A system and method for designing a broadband tuner such that VCO pulling is minimized and gaps in frequency coverage are avoided, while total power consumption is reduced, is disclosed. A broadband spectrum is divided into sub-bands and various multipliers to a local oscillator output are introduced. In this fashion, the present invention allows a local oscillator within the broadband tuner to always generate signals that lie outside of the broadband spectrum for a particular broadband application. Additionally, a modulus ratio for a dual modulus prescaler with the local oscillator is maximized, thereby reducing power consumption.

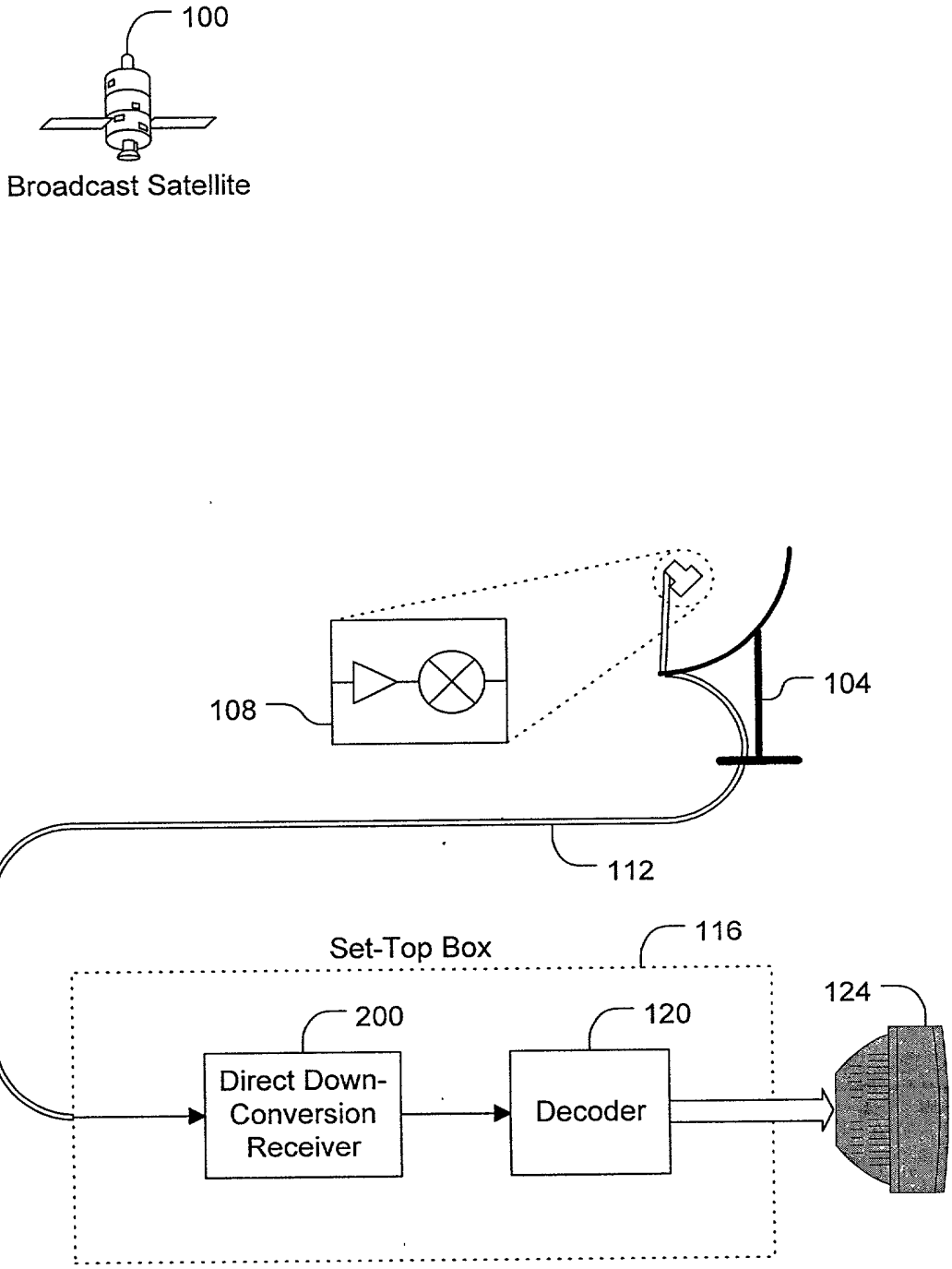
100
Broadcast Satellite
108
104
112
Set-Top Box
116
200
120
124
Direct Down-Conversion Receiver
Decoder

Fig. 1

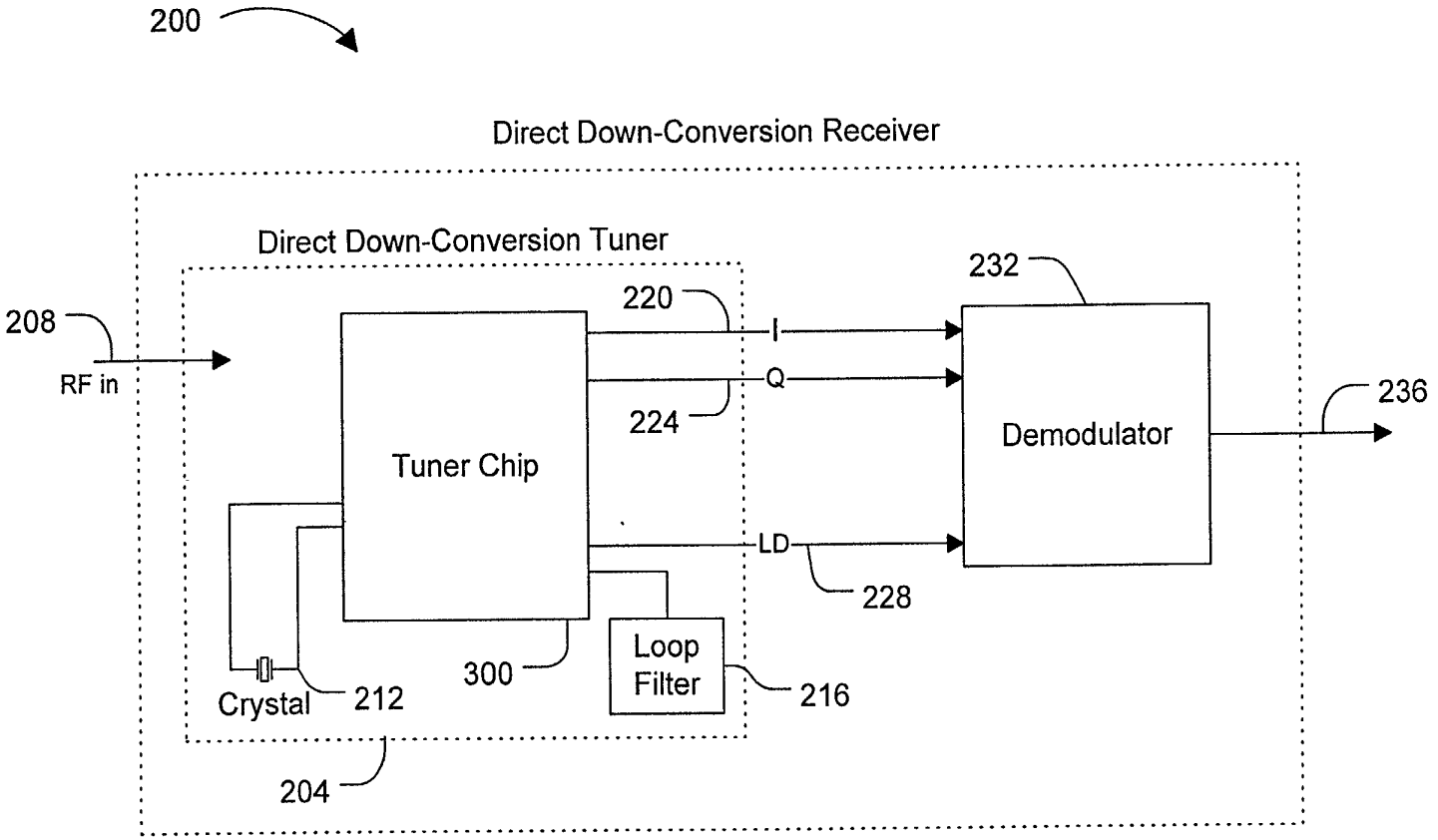
200
Direct Down-Conversion Receiver
Direct Down-Conversion Tuner
208
RF in
220
I
Q
224
232
Demodulator
236
Tuner Chip
LD
228
Loop
Filter
216
300
Crystal
212
204

Fig. 2

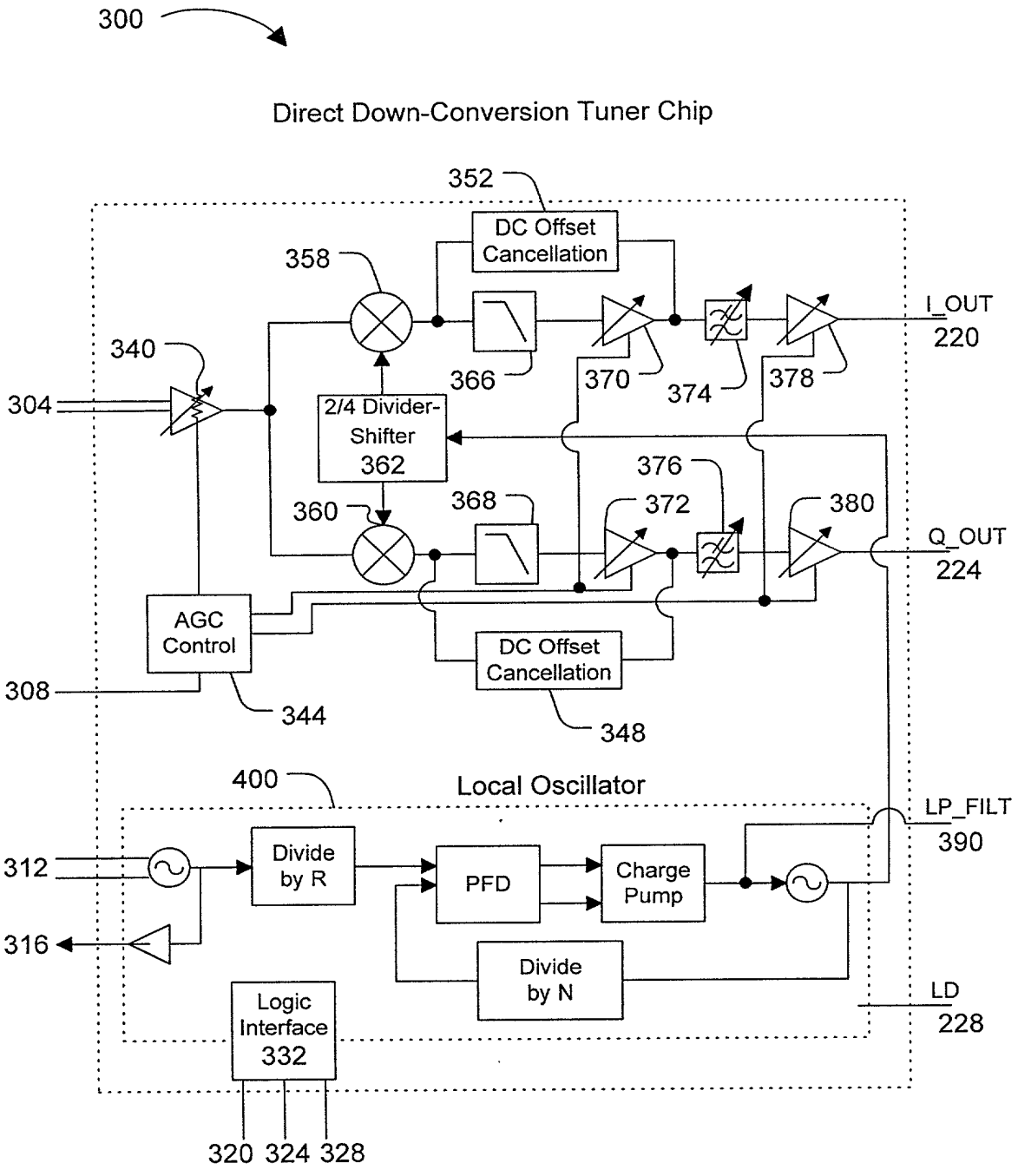
300
Direct Down-Conversion Tuner Chip
352
DC Offset Cancellation
358
340
304
366
370
374
378
I_OUT
220
2/4 Divider-Shifter
362
376
360
368
372
380
Q_OUT
224
AGC Control
308
344
DC Offset Cancellation
348
400
Local Oscillator
LP_FILT
390
312
Divide by R
PFD
Charge Pump
316
Divide by N
LD
228
Logic Interface
332
320
324
328

Fig. 3

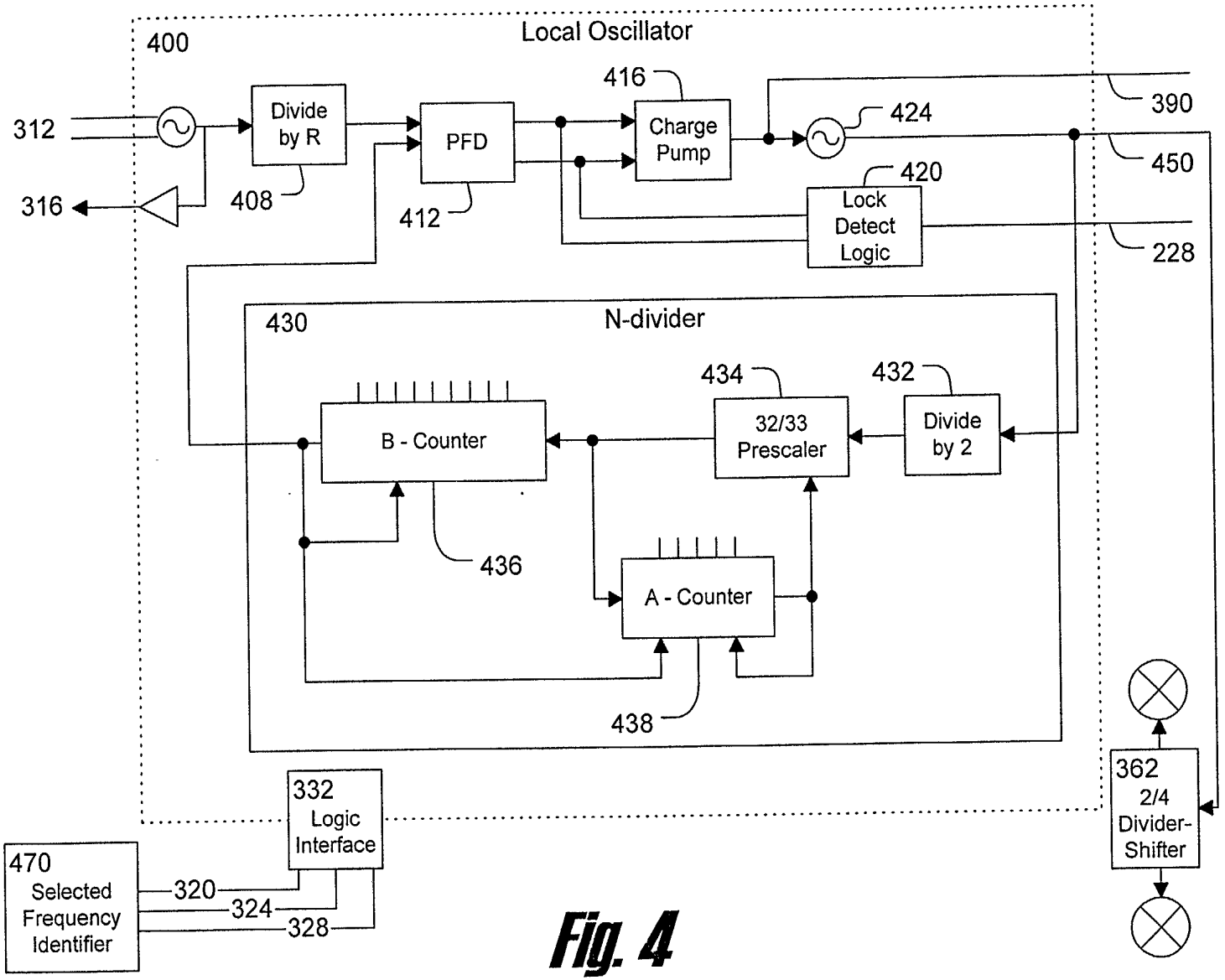
400
Local Oscillator
312
316
Divide by R
408
PFD
412
416
Charge Pump
424
390
450
420
Lock Detect Logic
228
430
N-divider
434
32/33 Prescaler
432
Divide by 2
B - Counter
436
A - Counter
438
362
2/4 Divider-Shifter
332
Logic Interface
470
Selected Frequency Identifier
320
324
328

Fig. 4

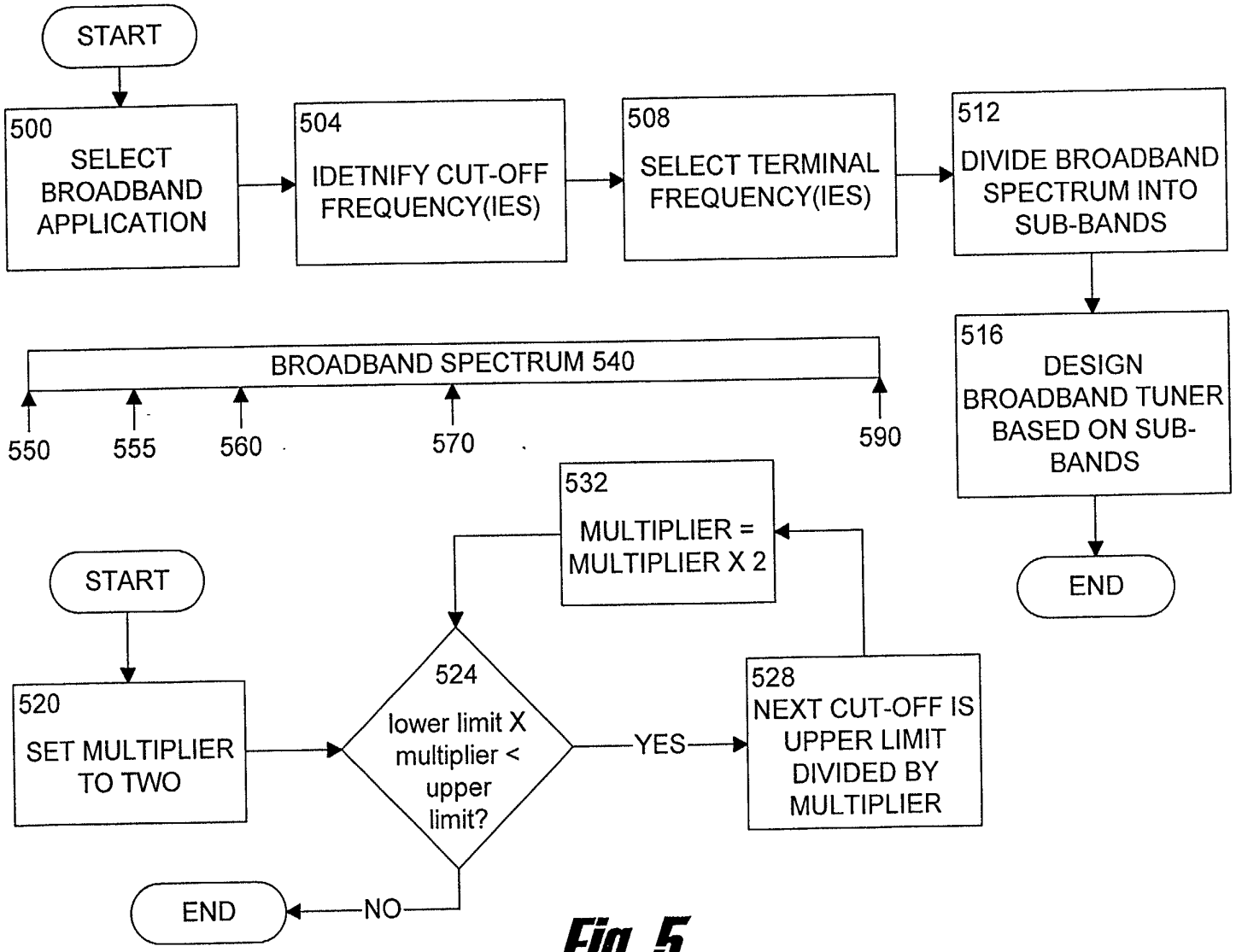
START
500
SELECT BROADBAND APPLICATION
504
IDETNIFY CUT-OFF FREQUENCY(IES)
508
SELECT TERMINAL FREQUENCY(IES)
512
DIVIDE BROADBAND SPECTRUM INTO SUB-BANDS
516
DESIGN BROADBAND TUNER BASED ON SUB-BANDS
END
BROADBAND SPECTRUM 540
550
555
560
570
590
532
MULTIPLIER = MULTIPLIER X 2
START
520
SET MULTIPLIER TO TWO
524
lower limit X multiplier < upper limit?
YES
528
NEXT CUT-OFF IS UPPER LIMIT DIVIDED BY MULTIPLIER
END
NO

Fig. 5

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248/002

UTILITY DECLARATION AND POWER OF ATTORNEY
Utility Application

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **SYSTEM AND METHOD OF FREQUENCY SYNTHESIS TO AVOID GAPS AND VCO PULLING IN DIRECT BROADCAST SATELITE SYSTEMS** the specification of which

(Check One)
☒ is attached hereto OR
☐ was filed on _____ as United States Application Serial No. SerialNumber or PCT International Application No. _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Date of Filing	Priority Claimed Yes	Priority Claimed No

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below.

Application Number(s)	Filing Date

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s), or § 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. Parent Application Number	PCT Parent Number	Parent Filing Date	Status-Patented, Pending or Abandoned

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248/002

POWER OF ATTORNEY: As a named inventor, I hereby appoint as my attorneys and/or agents, with full power of substitution and revocation, to prosecute this application and transact all business in the United States Patent and Trademark Office, and in countries other than the United States, and to do all things necessary or appropriate therefor before any competent International Authorities in connection with any international patent application(s) corresponding to the above-identified invention application, Daniel N. Yannuzzi, Reg. No. 36,727, and Semion Talpalatsky, Reg. No. 35,380, of CONEXANT SYSTEMS, INC., 4311 Jamboree Road, Newport Beach, CA 92660, and all of the registered practitioners identified by Customer Number 22249:

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Please send all correspondence to the attention of **Troy M. Schmelzer**, and direct all telephone calls to **(858) 552-8400 x 5565, facsimile (213) 955-0440.**

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Title 18, United States Code, § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

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INVENTOR'S SIGNATURE				DATE 6/6/2000	